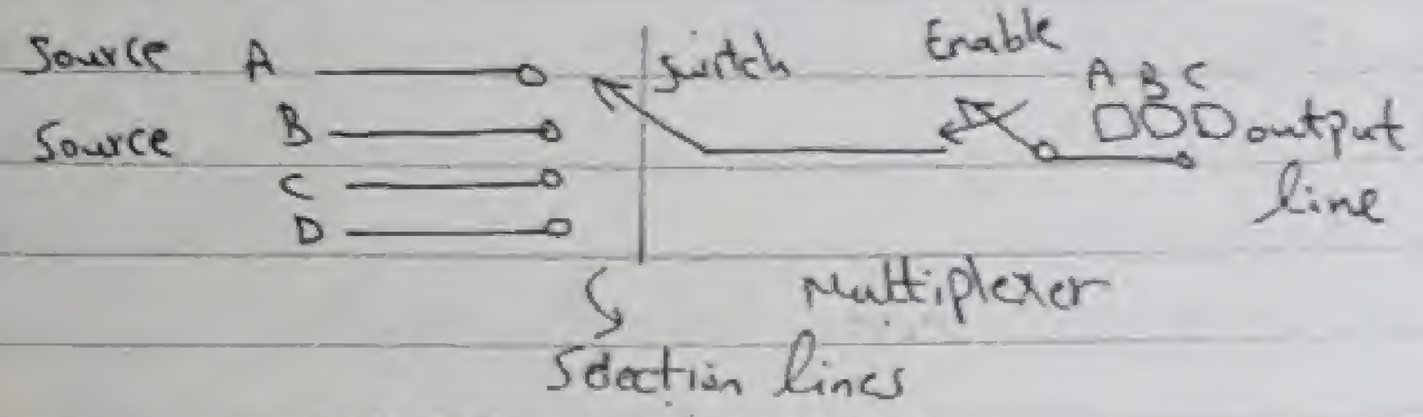
lec (5)
25/10/2016

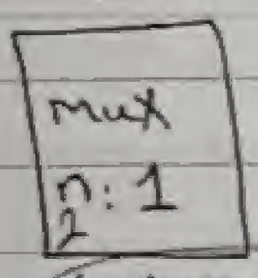
Combinational logic Circuit
"Data processing Circuits"

*Multiplexer



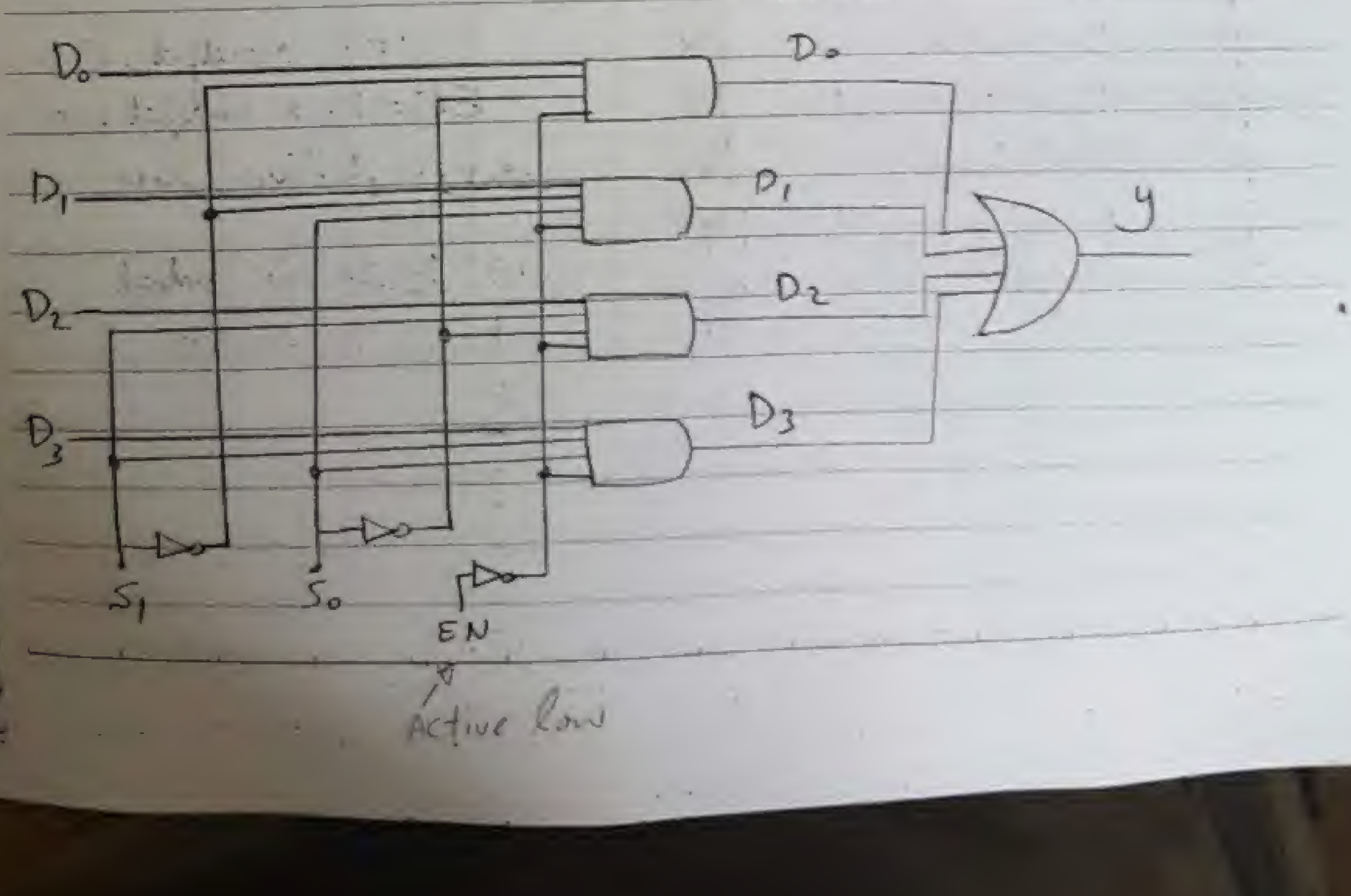
* يستخدم هذا الـ Multiplexer في الـ Time Division Multiplexing (TDM)
* يتكون الـ multiplexer من مجموعة من AND gates

Number of Source $\longrightarrow n \longrightarrow 2^n$ output $\longrightarrow 1$



4x1 Multiplexer ← AND gate يدخل لها (input) Source كل
(2 Selection lines)

Logic Circuit of Mux



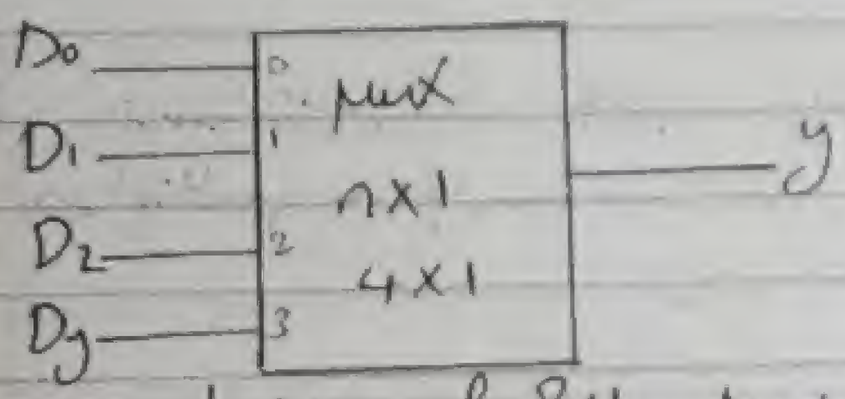
- 8x1 multiplexer, 3 selection lines

8 → AND gates

* Function table of 4x1 Mux

S_1	S_0	y
0	0	D_0
0	1	D_1
1	0	D_2
1	1	D_3

*logic symbol



* Function table of 8x1 Mux

EN	S_2	S_1	S_0	y
ϕ	0	0	0	D_0
1	0	0	1	D_1
1	0	1	0	D_2
1	0	1	1	D_3
1	1	0	0	D_4
1	1	0	1	D_5
1	1	1	0	D_6
1	1	1	1	D_7
0	X	X	X	0

EN = 0 → output = 0

EN = 1 → output = 1

* EN Active high

EN = 0 → output = 1

EN = 1 → output = 0

* EN Active low

EN	S_2	S_1	S_0	output
1	X	X	X	0
0				
0				
0				
0				

→ Sum of Product

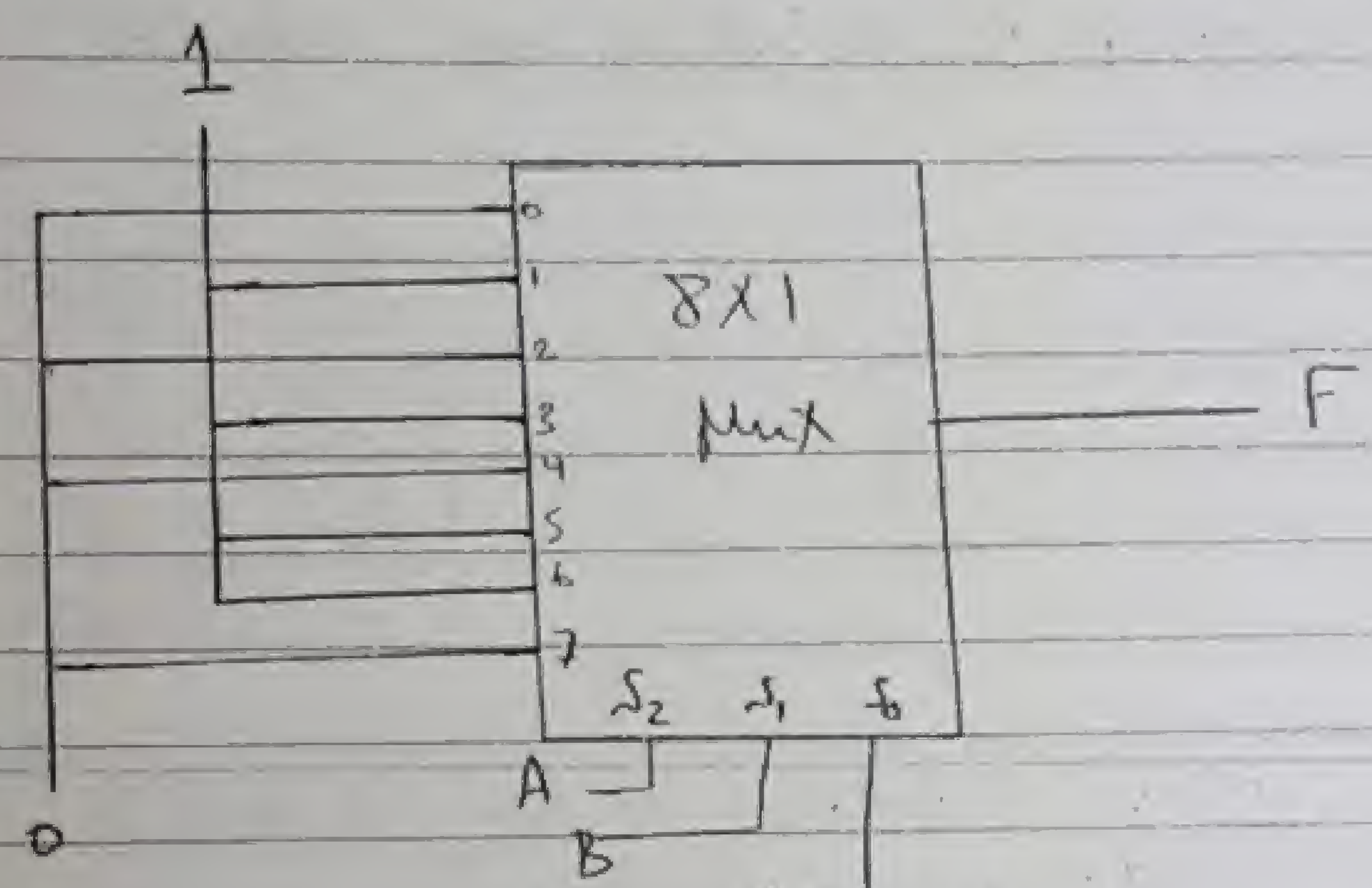
* $F(A,B,C) = \sum m(1,3,5,6)$ القيم اللي عندها F بواحد.

↳ minterm

Implement F using 8:1 multiplexer.

$F(A,B,C) = \bar{A}\bar{B}C + \bar{A}BC + A\bar{B}C + AB\bar{C}$ → من truth table

2^n inputs

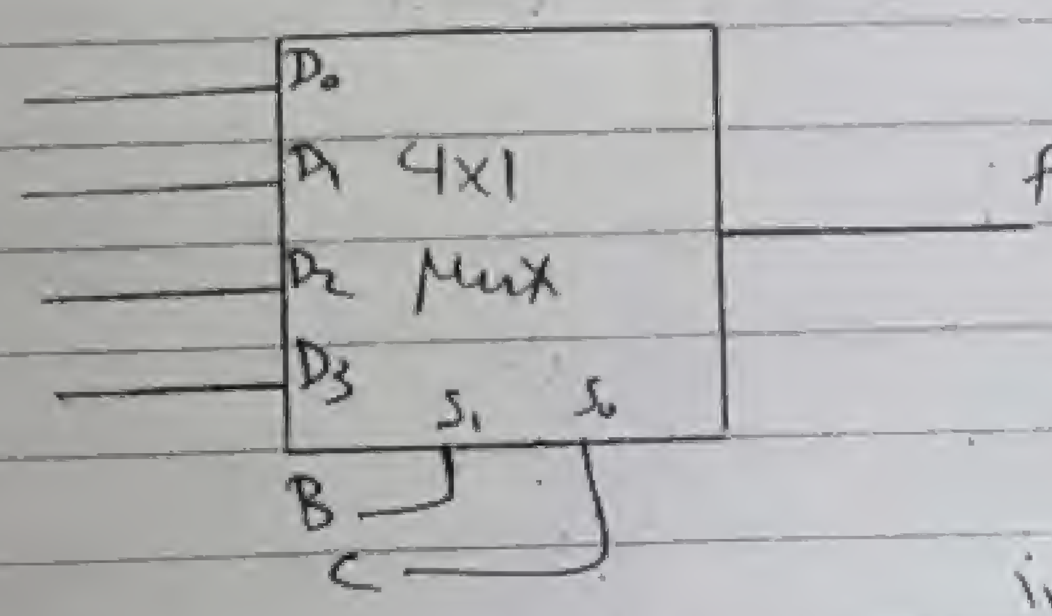


↳ n selection lines

* Implement the previous Function using 4X1 mux.

← هنا فدا ال selection هنعمل ك input لل mux كدة n المطلوبة

يساوي 2 فقط.



$F = \sum m(1,3,5,6)$

* طريقة تحديد ال inputs

① نضع دائرة على الارقام المقابلة minterms.

② ال inputs اللي مهندوش دوائر ← صفر واللي عنده دائرة ← واحد.

الدائرة التي تمثل $A \leftarrow A$

الدائرة التي تمثل $\bar{A} \leftarrow \bar{A}$

	D_0	D_1	D_2	D_3
$\bar{A}$	0	(1)	2	(3)
A	4	(5)	(6)	7
	0	1	A	$\bar{A}$

* طريقة أخرى باستخدام A,B ⇐ Selection

	$\bar{C}$	C
D_0	0	(1)
D_1	2	(3)
D_2	4	(5)
D_3	(6)	7

ملاحظة $F(A,B,C,D) = \text{-----}$

using 8x1 multiplexer

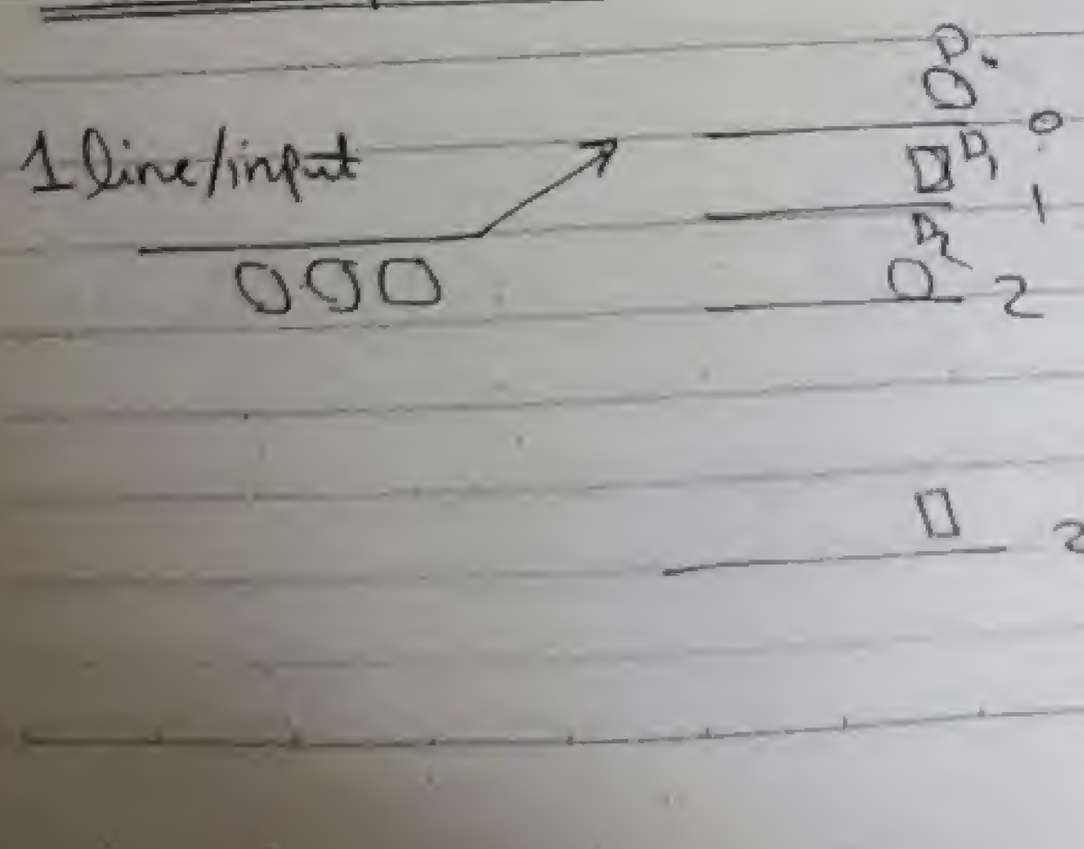
$B, C, D \rightarrow$ selection lines

$A \Rightarrow$ نفس الطريقة السابقة

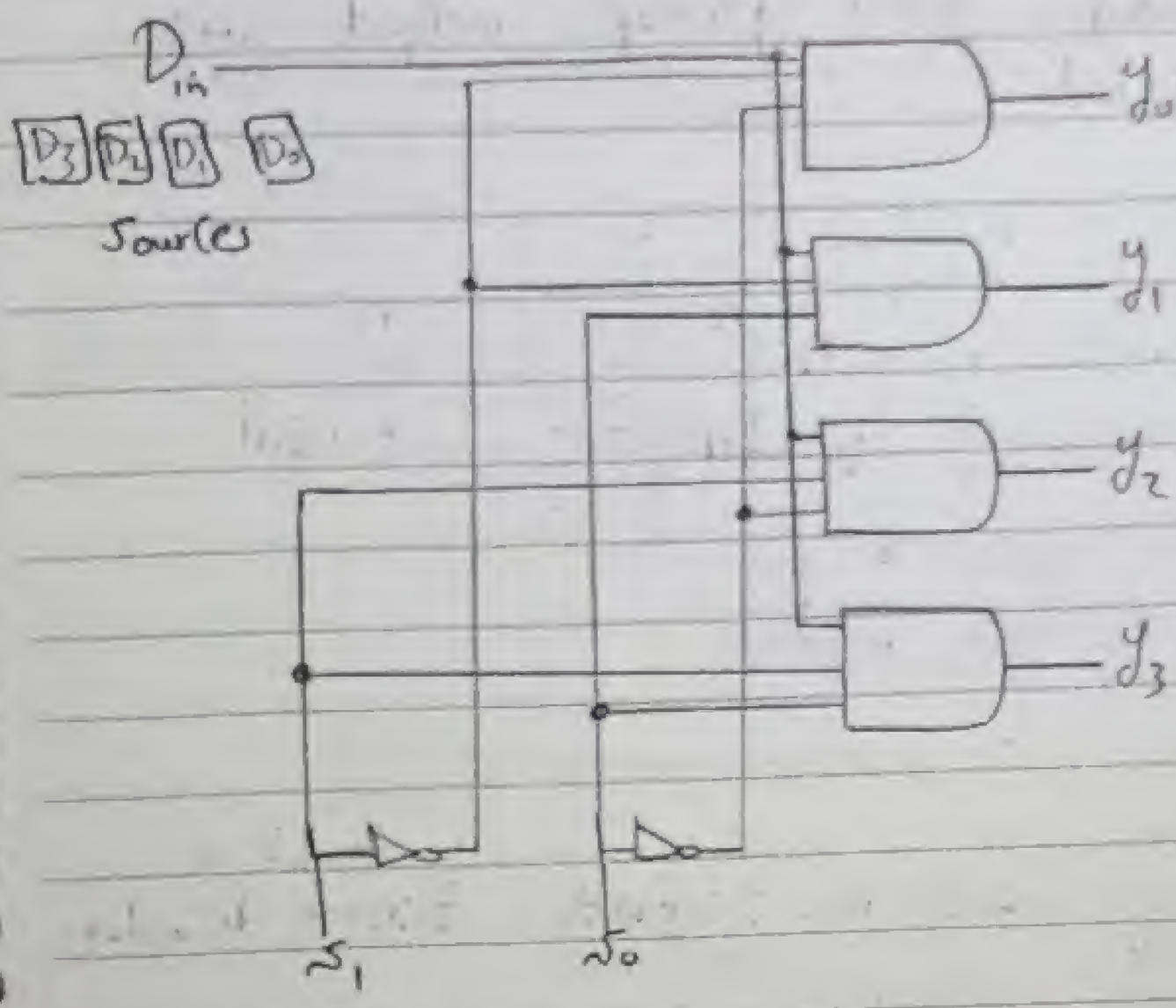
أو طريقة أخرى باستخدام function table multiplexer

74xx151 → (8x1 mux)

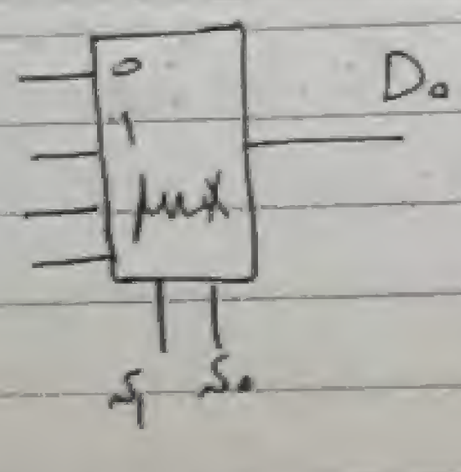
* Demultiplexer :-

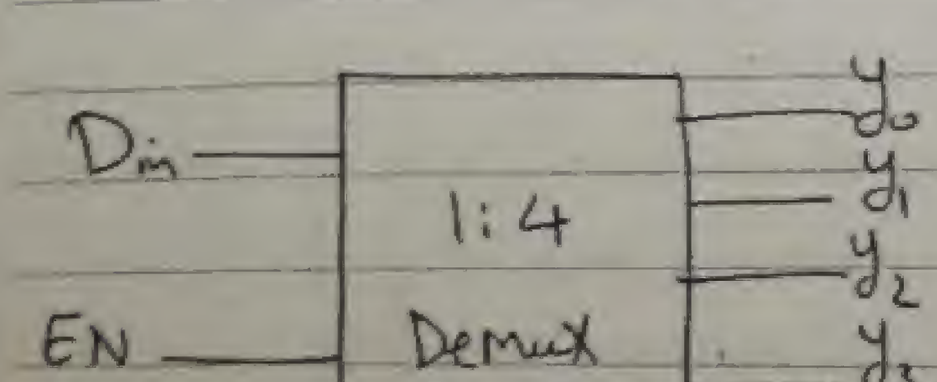


* Logic Circuit of 1X4 Demux

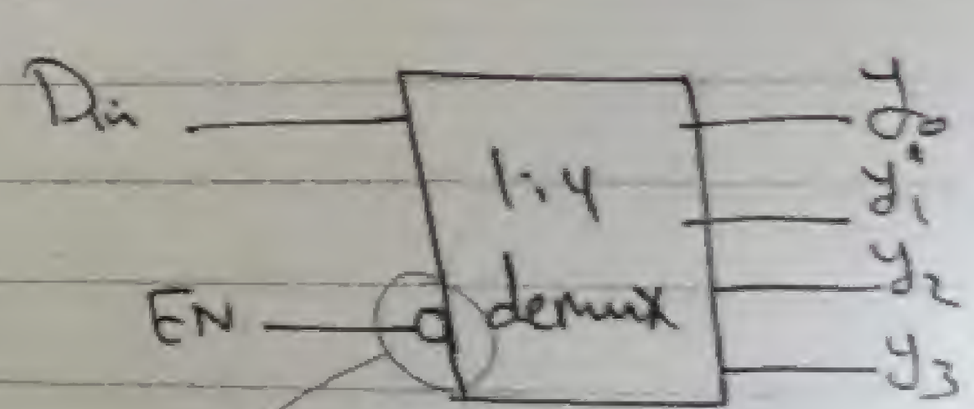


* Symbol





EN → Active high



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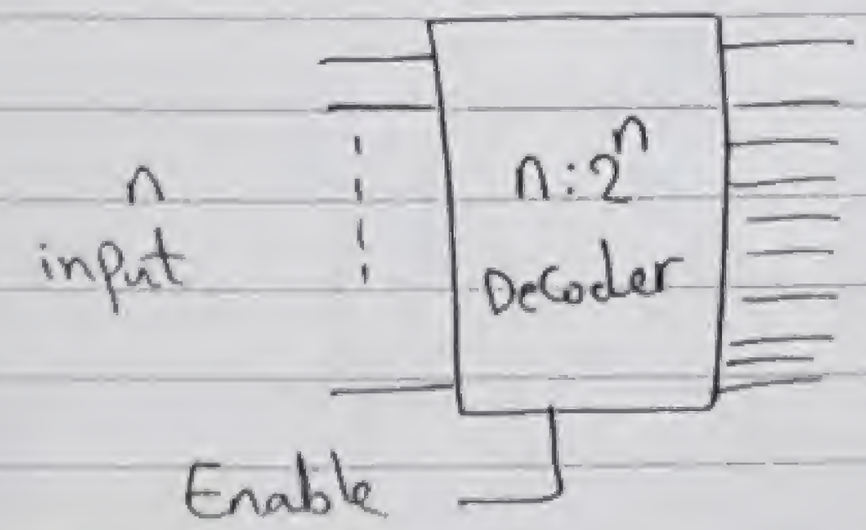
* Mux → Multiple input , Single output logic Circuit.

* Decoders Multiple input , Multiple output logic Circuit

تستغيز الداتا وبيتفرم في Security



ABC → 0000 0000
000

* انواعه :-
2 Binary decoder 2 Seven Sigment 2 octal decoder

* ملاحظه مهمه Selection lines

⊛ Function table of Decoders (2:4 line decoder)
(Active high Decoder).

A	B	D_0	D_1	D_2	D_3
0	0	1	0	0	0
0	1	0	1	0	0
1	0	0	0	1	0
1	1	0	0	0	1

Circuit Diagram ← AND gate يتكون من

Code word
01 → 0100
10 → 0010
11 → 0001

Active low ——uses——→ NAND gate in Circuit diagram.

* octal Decoder
3:8 line Decoder (8 AND gate ؟لـزم)